

REMARKS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

After entry of the foregoing amendment, Claims 1-20 are pending in the present application. Claims 1, 4-5, 8, 12-17, 18, and 19-20 are amended without introduction of new matter and Claims 2-3, 6-7, and 9-10 are canceled without prejudice or disclaimer by the present amendment.

In the outstanding Office Action, Claims 1-20 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite; Claims 16-19 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement; Claims 1, 2, 8, 11, 13, 14, and 20 were rejected under 35 U.S.C. § 102(b) as anticipated by JP 10-284574; Claims 1, 2, 8, 11, 13, 14, and 20 were rejected under 35 U.S.C. § 102(b) as anticipated by JP 7-171478; Claims 3, 4, 6, 7, 9, and 10 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP 10-284574; Claims 3, 4, 6, 7, 9, and 10 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP 7-171478; Claims 12 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP 10-284574; Claims 12 and 15 were rejected under 35 U.S.C. § 103(a) as unpatentable over JP 7-171478; and Claims 16-19 were indicated as allowable if rewritten to overcome their rejection under 35 U.S.C. § 112, second paragraph.

Applicants thank Examiner Jarrett for the indication of allowable subject matter.

Regarding the rejections under 35 U.S.C. § 112, first and second paragraphs, summarized above, the claims have been rewritten in view of the Examiner's comments. Accordingly, Applicants respectfully request that those rejections be withdrawn. Further, as Claims 16-19 are believed to overcome those rejections, Applicants respectfully submit that those claims are in condition for allowance.

Addressing now the remaining rejections of independent Claims 1 and 20 and the claims depending therefrom, summarized above, those rejections are respectfully traversed.

Amended Claim 1 is directed to a substrate processing system for processing substrates. The system includes:

first to n-th processing unit groups, n being a positive integer, each unit group having at least one processing unit and being configured to perform first to n-th substrate processing for given periods t1 to tn, respectively;

a loading/unloading section;

a first transfer section configured to receive/transfer the substrates from/to the loading/unloading section and to transfer the substrates one by one to one of the processing unit groups; and

a controller configured to control the first transfer section and the processing units such that each processing unit processes a substrate in a respective process time that is less than or equal to a standard one-cycle time, the one-cycle time being a maximum period among periods t1/m to tn/m, m being a positive integer equal to the processing units actually present in each of the first to n-th processing unit groups, respectively,

wherein the processing time of each processing unit includes a pre-transfer time, a net processing time, a post-transfer time, and a waiting time, and the controller adjusts the processing time of each processing unit in accordance with the one-cycle time.

As recited, the controller adjusts the processing time in accordance with the one-cycle time. Further, the processing time for each processing unit includes a pre-transfer time, a net processing time, a post transfer time, and a waiting time. Amended independent Claim 20 is directed to a method reciting a similar one-cycle time and processing time. The remaining claims depend from Claim 1, are cancelled, or are indicated as allowable.

In a non-limiting example, an embodiment of the present invention is described with respect to Figures 1-5. Referring to Figure 1, a substrate processing system removes substrates, one by one, from a cassette CR to processing section 3 having a plurality of processing units stacked as shown in Figure 3.¹ The wafers are transferred from processing

¹ Specification, page 7, lines 14-22; page 8, lines 7-10.

section 3 to a main-arm 7, which transfers a wafer to any processing unit of the system, via an extension unit EXT and alignment unit ALIM.²

Each processing unit can process a substrate for, at most, a maximum processing time of one cycle.³ The maximum processing time Tmax is determined by dividing the time required for each type of process by the number of processing units allocated thereto, respectively, and further taking the longest duration of those calculated values for each type of process.⁴ For instance, if the time for developing is tDEV and two identical processing units are allocated to developing, then the processing time for each developing unit is tDEV divided by two.⁵

The maximum processing time Tmax can then be used to determine the processing time of other processing units (e.g., units other than those by which Tmax was calculated). The pre-transfer, net-processing, and post-transfer times of the other processing units may set, for example, as follows: (pre-transfer time) + (net processing time) + (post-transfer time) < Tmax (one cycle).⁶

For instance, if an exposed substrate is transferred to a post-exposure baking processing unit PEBAKE, there is a risk that the substrate will be over-baked if it remains in that processing unit PEBAKE for too long. In a non-limiting example, the embodiment illustrated in Figure 8 addresses this problem by lifting the post-exposure substrate from the hot plate 104, via lift pins 101, for a pre-waiting time, to protect against over-baking.⁷ The pre-waiting time (e.g., time on the hot plate 104) is determined in part based on Tmax.⁸

The outstanding Office Action cites JP10-d284574 and JP 7-171478 as teaching the features of independent Claim 1 as originally filed. However, neither of those references

² Specification, page 8, line 11 – page 9, line 1.

³ Specification, page 14, lines 35-37.

⁴ Specification, page 14, line 35 – page 15, line 17.

⁵ Specification, page 15, lines 7-12.

⁶ Specification, page 15, lines 18-26.

⁷ Specification, page 19, lines 18-28.

⁸ Specification, page 19, lines 29-32.

teaches the claimed determination of a one-cycle time used for adjusting processing times; and neither reference teaches a controller that adjusts a processing time in accordance with a one-cycle time. Further, neither reference teaches a processing time for each processing unit that includes a pre-transfer time, a net processing time, a post transfer time, and a waiting time.

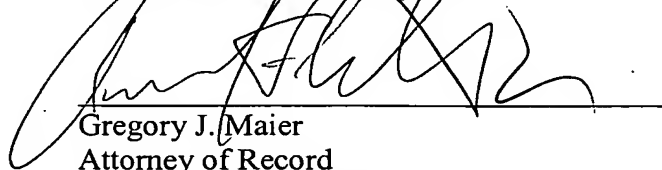
Applicants note, since the claimed controller adjusts the processing time of each processing unit in accordance with the one-cycle time, a processing time of a processing unit can be adjusted while a substrate remains within the processing unit. Thus, because the controller is not solely limited to adjusting the processing time by adjusting a transfer time of a transfer section, it is unlikely that the substrate will be subjected to a temperature change during adjustment of a processing time. On the other hand, both JP 10-284574 and JP 7-171478 teach the adjusting of a processing time by adjusting a transfer time of a transfer section. Further, a substrate is likely subjected to a temperature change by that adjustment.

Accordingly, for the reasons stated above, Applicants respectfully request that the rejections of independent Claims 1 and 20, and the claims depending therefrom, be withdrawn.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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